REMARKS/ARGUMENTS

Claims 1-28 are pending in the application. Claims 1-28 stand rejected in the Advisory Action mailed October 3, 2007 and under 35 U.S.C. § 103(a) in the Final Office Action, mailed June 5, 2007. Claims 3-4, 11, 17 and 23 are cancelled.

35 U.S.C. § 103(a) Rejection

Shiell does not teach "to determine the width of said execution unit"

Claims 1-28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shiell et al., U.S. Patent Number 5,913,049, (hereinafter "Shiell"). Although Examiner has presented her rejection in the form of an obviousness rejection, it appears that Examiner is actually making an anticipation argument. Examiner has not stated that applicants' claims are rendered obvious by a combination of references, but has instead asserted that a single reference explicitly teaches some elements of applicants' claims and inherently teaches others. Therefore, applicants respectfully request the Examiner clarify her rejection. In the present response, applicants will address Examiner's arguments that the claim element of "wherein said multi-thread scheduler is to determine the width of said execution unit" is inherent in the Shiell reference.

An "anticipating" reference must describe all of the elements and limitations of the claim in a single document, and enable one of skill in the field of the invention to make and use the claimed invention. *Merck & Co., Inc. v. Teva Pharmaceuticals USA, Inc.*, 347 F.3d 1367, 1372 Cir. 2003). A claim limitation is inherent in the prior art if it is necessarily present in the prior art, not merely probably or possibly present. *Akamai*

Technologies, Inc. v. Cable & Wireless Internet Services, Inc., 344 F.3d 1186, 1192-1193 (Fed. Cir. 2003).

On page 5 of the Office Action dated June 5, 2007, Examiner states:

> it is obvious that the width of the execution unit is been taking into consideration by the scheduler because each thread/instruction may require more or less bandwidth of the execution unit because Shiell clearly discloses that schedule logic 60 compiles all information from these Aops and microcode instructions and decides which instructions to launch to the execution units, in which order.

Emphasis in original.

The mere assertion that schedule logic compiles "all information" does not enable one of ordinary skill to practice applicants' claimed invention. Additionally, "all information" does not "necessarily" include the width of an execution unit, as would be required under the case law to show anticipation. In fact, the portion of Shiell cited by Examiner states "all information from these Aops and microcode instructions . . . ." Emphasis added. The information the specification is referring to is information relating to instructions, not information relating to an execution unit. Therefore, "all information" as used in Shiell clearly does not include the width of an execution unit.

The specification of Shiell discusses a scheduler that schedules instructions based on dependency check logic to avoid resource conflicts and a set of priority determinations that include scheduling microcode instructions before scheduling non-microcode AOps. *See e.g.* column 9, lines 13-21. Each execution unit has an associated queue where the scheduler sends the instructions before they are executed. *See* Fig. 3, element 66. Because the scheduler utilizes multiple execution units, the bandwidth of any particular execution unit is not relevant to where an instruction is assigned. Therefore, Examiner's

statement that "the width of the execution unit [has] been tak[en] into consideration by the scheduler because each thread/instruction may require more or less bandwidth of the execution unit . . ." is not at all supported by the specification of Shiell.

Additionally, Shiell does not disclose having a single execution unit execute two threads in parallel, but instead teaches having two different execution units execute two different threads. The parallelism discussed in Shiell is the product having multiple execution units simultaneously executing threads, not having a single execution unit simultaneously executing multiple threads.

Applicants, therefore, assert that for at least all the reasons mentioned above, claims 1-28 are allowable. Accordingly, applicants request that the rejection under 35 U.S.C. § 103(a) be withdrawn.

The Claims Have Been Amended to Further Distinguish Between Shiell

The claims of the present invention have been amended to include the limitation of an in-order processor. The invention disclosed in Shiell clearly relates to an out-of-order processor.

> As shown in FIG. 1, microprocessor 10 is of the superscalar type, and thus includes multiple execution units. These execution units include two ALUs 42.sub.0, 42.sub.1 for processing conditional branch, integer, and logical operations, floating-point unit (FPU) 31, two load-store units 40.sub.0, 40.sub.1, and microsequencer 48.

Shiell 4:59-64. Applicants, therefore, assert that for at least all the reasons mentioned above, Shiell does not anticipate claims 1-28 as amended. Accordingly, applicants request that the rejection under 35 U.S.C. § 103(a) be withdrawn.

It is believed that this Response places the application in condition for allowance, and early favorable consideration of this Response is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the telephone number listed below.

The Office is hereby authorized to charge any fees, or credit any overpayments, to Deposit Account No. **11-0600**.

Respectfully submitted,
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